Design and Analysis of Low Cost IC Package Solution for 10 Gbit/s Applications

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***Abstract* — Low cost IC package solution for 10 Gbit/s applications will be presented. The RF-LGA, laminate based CSP will be used. Design and analysis, in the frequency and time domains, of the RF-LGA will be demonstrated. Results show that RF-LGA package, with wirebond technology, could achieve the required electrical performance for 10 Gbit/s applications.**

I. Introduction

The explosive expansion of the internet is challenging the capacities of data communication systems. 10Gbit/s transmission networks have now been widely introduced as commercial available high-speed systems [1]. However, to reduce the interface cost and increase the number of applications, a compact, cost-effective and high-performance 10 Gbit/s transceiver system is needed.

On the other hand, the high frequency packaging technology becomes more important in the design of these high-speed/high-frequency devices, because packaging and its electrical effects become more significant as the operating frequency increases. Plastic packages are widely used for high frequency applications. However this technology has been limited to frequency below 3 GHz, due to the inductance of the bond wire and plastic material properties.

In this paper, low cost package solution for 10Gbit/s applications, using RF-LGA (Land Grid Array) laminate-based package, will be presented. Design and analysis in the frequency and time domain will be presented.

II. RF-LGA package

The RF-LGA is a laminate based Chip Scale Package (CSP). The package consists of a BT substrate 200 um thick with top and bottom metal layers of 25 um. The metalization is Ni/Au plated over Cu, and the chip is encapsulated with a mold compound 0.9 mm in height. The package size considered in this work is 5x5 mm with 0.5 mm lead pitch. A SiGe die with dimensions of 1.65x1.65 mm is attached to a grounded die pad on the top signal layer. Wire bonds are used to connect the die to metal pads on the top signal layer. The size and location of these pads as well as the placement and dimensions of the corresponding traces can be designed with a large degree of freedom. This allows the RF-LGA package to be designed with signal integrity in mind. Finally, interconnect to the bottom layer solder pads are made through metal Vias. A large circular ground pad is placed in the center of the bottom layer. These pads are solder mask defined to provide the necessary optimal solder joint reliability. Fig. 1 shows the top and bottom view of 6x6 mm 40 pins RF-LGA package.

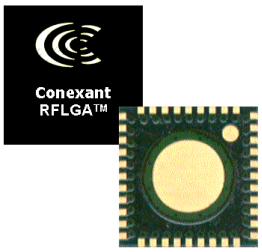

Fig. 1. 6x6 mm 40-pins RF-LGA package.

The measured loss associated with 6 cm 50 ohm microstrip metal line on the RF-LGA laminate substrate is less than 1 dB at 10 GHz. The metal traces on the top substrate layer can be extended close to the die edge to optimize the length of wirebonds and achieve better impedance matching for the package.

III. Design of RF-LGA package for 10 Gbit/s applications

Laser driver IC for 10 Gigabit Ethernet and SONET/SDH applications is placed into 5x5 mm RF-LGA package. Three set of differential signal work at 10 Gbit/s, the input, output, and clock signals. The differential data and clock inputs are used to minimize pattern dependent jitter, which is critical for the proper operation of the laser driver. The output signal drives 50 ohm differential impedance, which is 25 ohm for single line odd mode impedance. Although, the complete

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package is designed, the scope of this paper will be limited to the output section, for simplicity. The package parasitics should have minimal effects on the main characteristics of the wave propagating along the package leads.

The odd mode impedance of the output section is designed to be 25 ohm, using line width of 400 um on the laminate substrate thickness of 200 um. Two ac ground traces, width 100 um, are placed next to the signal traces at 75 um, to decrease the single line impedance from 40 ohm to 33 ohm, as shown in Fig. 2. The skin effect should be taken into consideration during the design of these metal line traces. It is clear that this configuration provides minimum variation in the line impedance across the broad frequency range of interest.

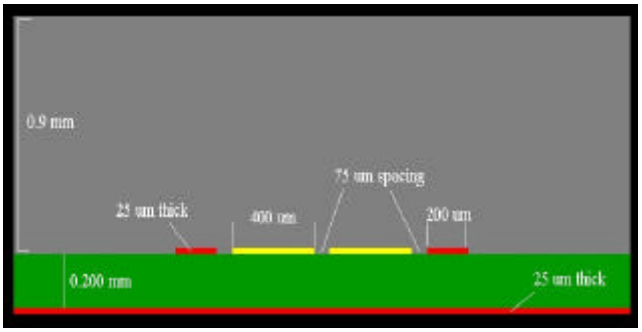

Fig. 2. Differential line with ground traces at both side. Data line and ground traces have 400 um and 200 um width, respectively. Substrate thickness is 200 um with epr=4.2.

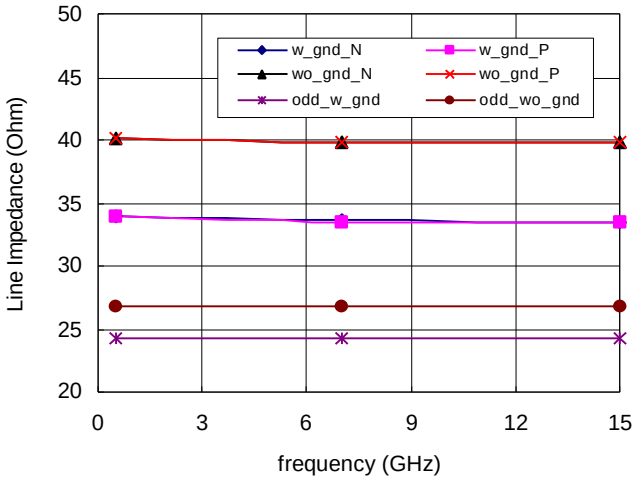

Fig. 3. Odd-mode line impedance and single-line impedance with and without ground traces at both sides.

The package layout is performed based on the results obtained from the line impedance calculation. An optimization among the metal traces length and the wirebonds length is performed. Several factors should be taken into consideration, the wirebond inductance and the loss in the laminate substrate. Fig. 4 shows the layout of the output section for two cases. The first with the optimized layout that consists of metal traces extended close to the die, and the second with no metal traces which represents the case of leadframe CSP.

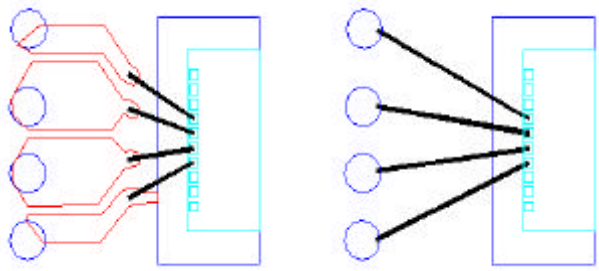

Fig. 4. Package output section layout for two cases, with metal traces and wirebonds, and with wirebonds only.

Table I presents the results of the inductance for both cases. It is obvious that the first case with metal traces and wirebonds has an effective inductance that equals to 0.6 nH compared to 0.8 nH for leadframe type of CSP. The RF-LGA package has about 25% less parasitic inductors compared to leadframe type CSP. Thus RF-LGA CSP provides less parasitics, and should have less effect on the electrical performance of the 10 Gbit/s laser driver performance.

TABLE I
INDUCTANCE VALUES FOR TWO CSP CASES – WIREBOND AND METAL TRACES AND WIREBOND ONLY

Inductance (nH)	vcca1	outP	outN	vcca2
	Wirebond Only			
vcca1	1.41	0.44	0.24	0.16
outP	**0.44**	**1.27**	0.37	0.22
outN	0.24	0.37	**1.21**	**0.38**
vcca2	0.16	0.22	0.38	1.24
	Metal Traces &Wirebond			
vcca1	1.25	0.41	0.24	0.17
outP	**0.41**	**1.04**	0.35	0.23
outN	0.24	0.35	**1.00**	**0.37**
vcca2	0.17	0.23	0.37	1.07

IV. Time domain simulation for 10 Gbit/s RF-LGA package

Traditionally, transmission line is modeled by cascading resistors, inductors and capacitors lumped elements. This method introduces a large number of nodes that substantially increases the simulation time. These lumped-element circuit models introduce excessive ringing and can give accurate results only within a limited frequency range. The lumped-element circuit models must be supplemented to account for frequency-dependent effects in transmission lines, such as skin effects and dispersion. Moreover, analytical model for lumped elements may not be accurate across broad frequency range, especially for coupled lines, which are critical parameters to evaluate cross-talk in high speed circuitry. In summary, s-parameters generated by measurement or high frequency simulation should be used directly in circuit simulation, especially for time-domain broad-band simulation.

An efficient frequency-domain modeling technique using scattering parameters has been developed. The method is based on a robust rational approximation algorithm. The algorithm generates multiport pole-residue models whose time-domain response can be efficiently calculated within circuit simulation. Once, the time domain response for the scattering parameters of specific circuitry is calculated, the results can be stored and used in future time domain simulation.

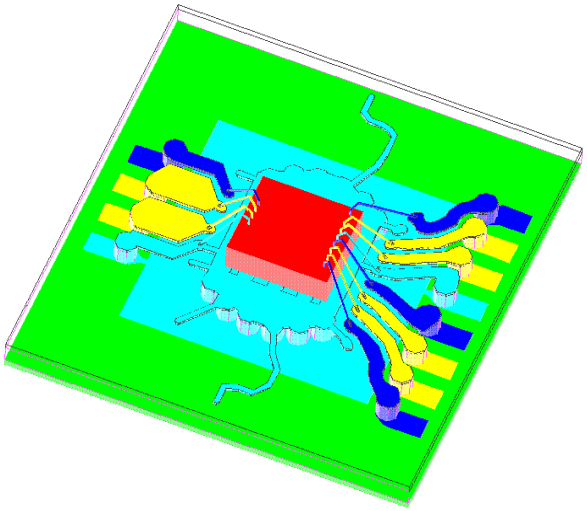

Fig. 5. Three-dimensional RF-LGA IC package layout with die connected to the package leads using wirebonds.

The three-dimensional layout of three set of differential pairs line on RF-LGA IC package for 10 Gbit/s laser driver is shown in Fig. 5. The output data lines are shown to the left, while the clock signal and input data lines are drawn to the right. These are the I/O of interest, since high speed signals will pass through them. The differential data lines are used to minimize pattern dependent jitter, that is critical for the proper operation of such high speed devices. The SiGe die has thickness of 0.33 mm. The die ground is connected to the bottom ground of the package through adequate number of Punch Thru VIAS (PTH). The package is mounted on Printed Circuit Board (PCB) with thickness of 0.8 mm and dielectric constant of 4.6. The dielectric constant of the laminate substrate is 4.2 with loss tangent of 0.009. The top mold compound has dielectric constant of 4.3, and no loss is assumed in the material.

The s-parameters for the I/O sections of interest is generated using electromagnetic simulation. In this paper, the output data lines are only considered. Fig. 6 presents the single line s-parameters, S11 and S21, for two cases, the signal lines with the edge coupled ground traces and without the ground traces. S33 and S34 should be the same due to the symmetry adopted in the design. Note that the ac ground traces are connected to ground, so only four-port s-parameters network is obtained from the simulation. The reflection coefficient is less than –15 dB at 10 GHz for the edge coupled ground case, which provide appropriate input matching conditions. The corresponding insertion loss is less than 1 dB at 10 GHz, which has been previously seen on microstrip line measured on the same substrate. The insertion loss for the edge coupled ground case is slightly less than the no-ground case due to the redistribution of the electric field line which in turn eases the discontinuity of the current singularity at the metal conductor edge.

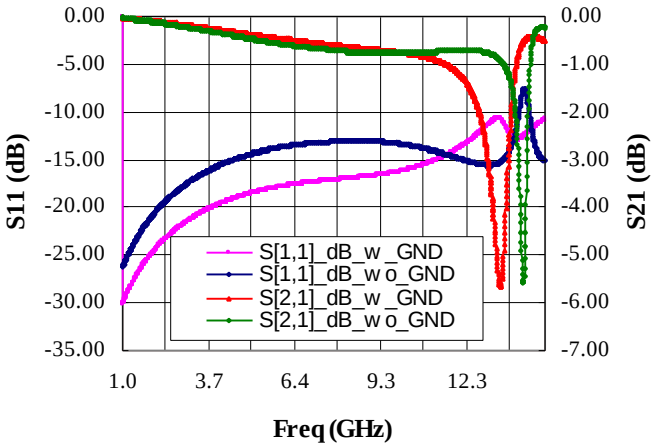

Fig. 6. Calculated s-parameters for the output data of the RF-LGA package with and witho10 Gbit/s crosstalk at the near and far end of the second signal trace. Input signal

amplitude is 300 mV with 10 ps rise time.ut the edge coupled ground traces.

The four-port s-parameters results are included in circuit simulation using 4-port network element. The rational approximation for the s-parameters is computed and converted into time-domain response. Fig. 7 shows the circuit configuration for transient analysis simulation. Two 10 ps rise time sources, with 25 ohm resistance, equal in amplitude and opposite in sign are placed at the input of the differential lines. The output is terminated by 25 ohm load at each line. This circuit will be used to evaluate the effect of the package parasitics on the electrical characteristics of the wave propagating through the package, such as signal distortion, overshoot, crosstalk, group delay, and settling time.

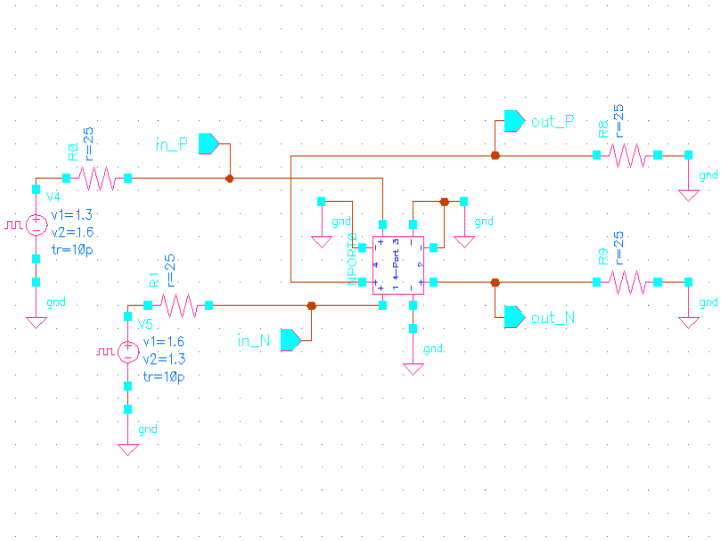

Fig. 7. Time-domain circuit simulation circuit for the output data lines using calculated 4-port s-parameters results.

V. Results and Discussion

Transient analysis, with duration of 0.5 ms, is performed for the circuit shown in Fig. 7 to evaluate the effect of the package parasitics on the electrical characteristics of the signal propagating along the output data lines. Fig. 8 shows the input/output waveform of the 300 mV amplitude and 10 ps rise time signal for the output data section. The overshoot is about 7.5% and the settling time equals to 70 ps. The rise time and group delay are 30 ps and 27 ps, respectively. Fig. 9 depicts the crosstalk signal at the near and far ends of one of the differential pair lines. The level of crosstalk signal is less than 10%, which is well within the acceptable range of digital lines.

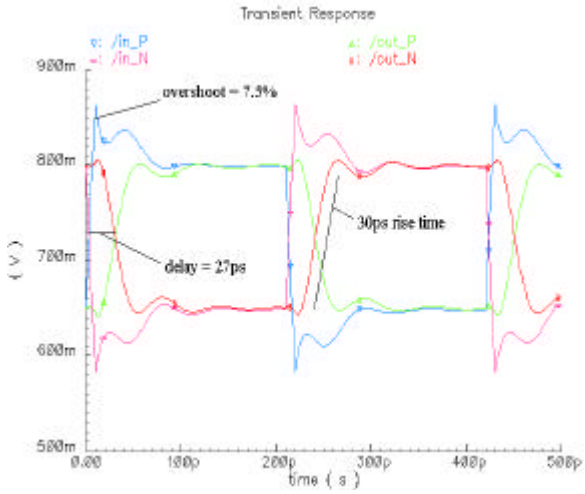

Fig. 8. 10 Gbit/s Input/output signal waveform for the output data section of the RF-LGA package. Input signal amplitude is 300 mV with 10 ps rise time.

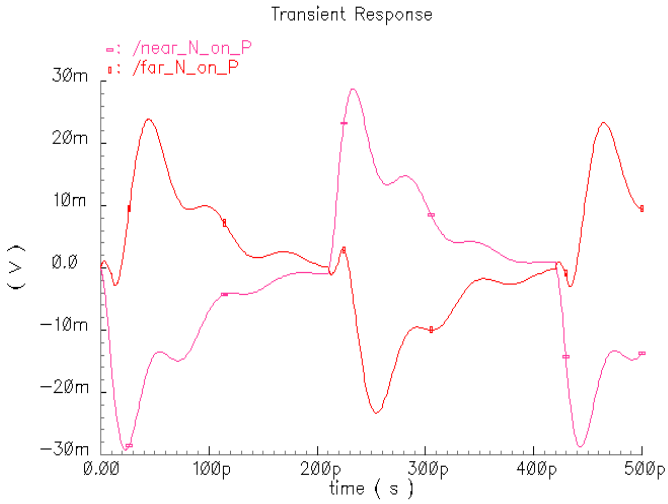

Fig. 9. 10 Gbit/s crosstalk at the near and far end of the second signal trace. Input signal is 300 mV with 10 ps rise time.

VI. Conclusion

Low cost IC package solution, based on RF-LGA package and suitable for 10 Gbit/s applications, is presented. The RF-LGA package is in production at the present time. Design trade off of the 10 Gbit/s package is depicted. Analysis and simulation in both the frequency and time domains is shown. The simulated s-parameters is directly used in the time domain simulation. Results show 7.5% overshoot, 70 ps settling time, 30 ps rise time, and 27 ps delay time with the input/output waveform.

REFERENCES

[1] T. Yamamot et Al., "High performance 10Gbit/s optical receiver using APD and highly integrated HBT Ics with PLL," *Electronics Letters.*, vol. 36, no. 2, pp. 158-159, Jan. 2000.